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EXAMINER	
FLOURNOY, HORACE L	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,897	MENON ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed August 7th 2006. Claims 1-24 are pending. Applicant's arguments have been carefully and respectfully considered, but they are not entirely persuasive, as will be discussed in more detail below, even in light of the instant amendments.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by **Kenner et al. (U.S. Patent No. 5,903,749 hereafter referred to as Kenner)**.

Independent Claims

With respect to **independent claims 1 and 22,**

(and dependent claim 19)

> *"A method comprising: executing a speculative read-reordered load instruction* **[Kenner discloses in column 1, lines 25-26, "...these compilers must be able to freely reorder the instructions to be effective. Also see the abstract]**

prior to a potentially conflicting load in an instruction sequence; **[disclosed, e.g. in FIG. 1, step 130. See column 11, lines 39-41]** *storing memory conflict information* **[Kenner discloses in the abstract, "storing memory conflict information"]** *representing the speculative* **["preload array entry" (column 4, line 16) / "preload instruction" (column 2, line 37). Also see "Other Publications" of Kenner]** *read-reordered load;* **[see limitation above]** *executing a read-reordered load check instruction associated with the speculative read-reordered load instruction, the read-reordered load check instruction to determine if an address of a the potentially conflicting load matches an address of the stored memory conflict information; and* **[Kenner discloses in the abstract, lines 16-18, "determining if a memory conflict has occurred between the first address and the second address using the previously stored memory conflict information."]** *validating the stored memory conflict information with a matching address to the address of the potentially conflicting load if the stored memory conflict information has a data value that is the same as a data value of the potentially conflicting load."* **[Kenner discloses this limitation in column 16, lines 36-45. The examiner notes that a valid bit can be used to either invalidate or validate a particular data item, depending on its setting. Additionally, Kenner discloses using the *same* data values of potentially conflicting loads when validating in column 19, lines 17-22.]**

[With further respect to claims 22-24, Kenner discloses in column 9, line 60 – column 10, line 3, "...software 335 for execution..."]

~~*invalidating the stored memory conflict information with a matching address to the address of the potentially conflicting load if the stored memory conflict information has a value different than a value of the potentially conflicting load.*~~

With respect to **independent claim 7,**

(and dependent claims 8, 17 and 19)

"A processor **[See FIG. 1, element 305]**, *comprising: a re-ordered load address table (RRLAT) to store memory conflict information representing a speculative read re-ordered load* **[FIG. 3, element 345: "Dynamic Memory Conflict Resolution Unit"]** *that is executed prior to a potentially conflicting load in an instruction sequence;* **[See FIG. 4, step 430 and all associated text within specification]**; *and a monitor* **[Kenner discloses a "conflict resolution circuit" in column 10, paragraph 5 and FIG. 3, element 392]** *to: compare a potentially conflicting load against the stored memory conflict information by executing a read-reordered load check instruction associated with the speculative read-reordered load instruction, the read-reordered load check instruction to determine if an address of the potentially conflicting load matches an address of the stored memory conflict information;* **[Kenner discloses in column 11, lines 9-12, "At step 420, the dynamic memory conflict resolution unit 345 determines whether a memory conflict occurred involving a register associated with the check no-invalidate instruction."]** *validate the stored memory conflict information with a matching address to the address of the potentially conflicting load if the stored memory conflict information has a data value that is the same as a data value of the potentially conflicting load."* ~~*invalidate the stored memory conflict information if the stored memory conflict information has a matching address and a different value than the potentially conflicting load*~~ **[Kenner discloses this limitation in column 16, lines 36-45. The examiner notes that a valid bit can be used to either invalidate or**

validate a particular data item, depending on its setting. Additionally, Kenner discloses using the *same* data values of potentially conflicting loads when validating in column 19, lines 17-22.]

With respect to **independent claim 16,**

"A computer system, comprising: a first processor; and a second processor, **[Kenner discloses in column 1, lines 19-26, "...for execution by one or more processors in the computer system...." Kenner also discloses in column 9, lines 55-58, "While this embodiment is described in relation to a single processor computer system, the invention could be implemented in a multi-processor computer system."]** *including: a re-ordered load address table (RRLAT) to store memory conflict information representing a speculative read re-ordered load received from the second processor that is executed prior to a potentially conflicting load in an instruction sequence;* **["...On certain processors (e.g., superscalar processors, very long instruction word processors, etc.), allowing the compiler to reorder the object code instructions can improve performance by exposing simultaneously executable instructions. However, these compilers must be able to freely reorder the instructions to be effective." Also see "Other Publications" of Kenner]** *and a monitor to: compare a potentially conflicting load received from the first processor against the stored memory conflict information, by executing a read-reordered load check instruction associated with the speculative read-reordered load instruction,* **[Kenner discloses in column 11, lines 9-12, "At step 420, the dynamic memory conflict resolution unit 345 determines whether a memory conflict occurred involving a register associated with**

the check no-invalidate instruction."] *the read-reordered load check instruction to determine if an address of the potentially conflicting load matches an address of the stored memory conflict information: and* **[Kenner discloses this limitation, e.g. in column 3, lines 28-35, 40-45, column 17, lines 51-57]** ~~*and to*~~ *validate the stored memory conflict information with a matching address to the address of the potentially conflicting load if the stored memory conflict information has a data value that is the same as a data value of the potentially conflicting load."* ~~*invalidate the stored memory conflict information if the stored memory conflict information has a matching address and a different value than the potentially conflicting load*~~ **[Kenner discloses this limitation in column 16, lines 36-45. The examiner notes that a valid bit can be used to either invalidate or validate a particular data item, depending on its setting. Additionally, Kenner discloses using the *same* data values of potentially conflicting loads when validating in column 19, lines 17-22.]**

With respect to **independent claim 18,**

"A computer system, comprising: a memory device; and a processor coupled to the memory device, **[See FIG. 1, element 305]**, *including: a re-ordered load address table (RRLAT) to store memory conflict information representing a speculative read re-ordered load that is executed prior to a potentially conflicting load in an instruction sequence;* **[See rejection of claims 1, 4, and 5]**; *a monitor to compare a potentially conflicting load against the stored memory conflict information by executing a read-reordered load check instruction associated with the speculative read-reordered load instruction, the read-reordered load check instruction to determine if an address of the potentially conflicting load matches*

an address of the stored memory conflict information: **[See rejection of claim 7]**, *and to validate the stored memory conflict information with a matching address to the address of the potentially conflicting load if the stored memory conflict information has a data value that is the same as a data value of the potentially conflicting load." ~~invalidate the stored memory conflict information if the stored memory conflict information has a matching address and a different value than the potentially conflicting load~~* **[Kenner discloses this limitation in column 16, lines 36-45. The examiner notes that a valid bit can be used to either invalidate or validate a particular data item, depending on its setting. Additionally, Kenner discloses using the *same* data values of potentially conflicting loads when validating in column 19, lines 17-22. Kenner discloses in column 17, lines 42-44, "...if a matching entry is found, then the valid indication of that entry is polled. If the valid indication is in the conflict/invalid state.]**; *and a cache memory;"* **[Kenner discloses in column 16, lines 25-26, "This table may be implemented using any form of cache." With respect to claim 18 Kenner discloses "" in FIG. 3, element 310, "Storage Device"]**

Dependent Claims

With respect to **claims 2, 8, 17 and 19,**

"The method of claim 1, further comprising validating the stored memory conflict information ~~with~~ having the matching address if the stored memory conflict information has ~~the same~~ a data value as different than the data value of the potentially conflicting load." **[Kenner discloses this limitation in column 17, lines 9-14]**

With respect to **claim 3,**

"The method of claim 2, wherein the validating of the stored memory conflict information of the read re-ordered load check instruction **[Kenner discloses this limitation, e.g. in column 3, lines 28-35.]** *further comprises passing control by the read re-ordered load check instruction to a next instruction in the instruction sequence."* **[Kenner discloses this limitation e.g. in column 15, lines 14-22. Kenner further discloses in column 6, lines 7-10 "...each iteration through the loop requires an entry to be created in the preload array in response to executing the preload instruction, as well as the invalidation of that entry in response to executing the check instruction."]**

With respect to **claim 4,**

"The method of claim 1, wherein the memory conflict information is stored in a read re-ordered load address table (RRLAT). " **[See FIG. 3, element 390 and column 8, paragraph 1. Kenner discloses in column 8, lines 10-12, "The memory conflict resolution unit includes a conflict resolution circuit coupled to a table."]**

With respect to **claims 5 and 19,**

"The method of claim 4, further comprising updating the stored memory conflict information by setting a validity bit **[Kenner discloses in column 3, lines 34-35, "...a valid bit indicating whether the entry currently contains valid data.]**, *in the RRLAT* **[See rejection of claim 4]** *to a valid state when new memory conflict information is stored."* **[Kenner discloses in column 11, lines 55-57, "The**

term validity indication is used to refer to any data (e.g., a bit, a string of bits) used to identify whether memory conflict information is valid."]

With respect to **claim 6,**

"The method of claim 5, further comprising setting the validity bit to an invalid state **["invalidated"]** *if a later conflicting load operation* **[See Tables 1A and 1B]** *is executed* **[See FIG. 1].** *"* **[Kenner discloses in column 4, lines 12-17, "If the conflict bit of this entry is set, then a memory conflict occurred and flow passes to step 140. Otherwise, flow passes to step 130...As shown in step 130, the preload array entry is invalidated by resetting its valid bit."]**

With respect to **claim 9,**

"The processor of claim 8, wherein the validating of the stored memory conflict information of the read re-ordered load check instruction further includes passing control by the read re-ordered load check instruction to a next instruction in the instruction sequence. **[Kenner discloses this limitation e.g. in column 15, lines 14-22. Kenner discloses in column 17, lines 42-44, "...if a matching entry is found, then the valid indication of that entry is polled. If the valid indication is in the conflict/invalid state. See also column 19, lines 5-29 and the rejection to claims 2 and 8]**

With respect to **claim 10,**

"The processor of claim 7, wherein the RRLAT **[See rejection of claims 1 and 4]** *is referenced* **[Note: RRLAT is part of element 345 of FIG. 3. See also the**

rejection to claims 4 and 5] *upon the execution of a read re-ordered load check instruction to determine the validity of the speculative read re-ordered load."* **[See rejection of claim 20 below]**

With respect to **claim 11,**

"The processor of claim 7, wherein the RRLAT **[See rejection of claims 1 and 4]** *may be any one of a direct-mapped, multi-way set associative* **[Kenner discloses in column 16, line 54, "set-associative"]**, *and fully associative data structure* **[See column 16, paragraphs 2-4]**." **[Kenner further discloses in column 16, lines 25-26, "This table may be implemented using any form of cache."]**

With respect to **claim 12,**

"The processor of claim 7, wherein the RRLAT **[FIG. 7 and also rejection of claims 1 and 4]** *is portioned among hardware thread contexts."* **[Kenner discloses in column 18, lines 3-7, "The dynamic memory conflict resolution unit 705 is shown including a table 710 for storing the memory conflict entries. Although only one storage area in the table 710 is being described, each of the storage areas in the table 710 has associated with it a set of comparators (740) and an AND gate (745). " The examiner interprets "hardware thread contexts" as analogous to comparators and an AND gate.]**

With respect to **claim 13,**

"The processor of claim 7, wherein the RRLAT **[See rejection of claims 1 and 4]** *includes storage locations for an address* **[Kenner discloses in column 18, lines 7-10, "Each memory conflict entry stored in table 710...]**, *a target register ID* **["...has a location identifier field (715),]**, *a value* **["...a signature field (720), a width field (722),]**, *and validity information associated with the speculative read re-ordered load."* **["...and a valid indication field (725). See FIG. 7, elements 710, 715, 720, 722, and 725]**

With respect to **claims 20 and 24,**

"The machine-readable medium of claim 23, wherein the validating of the stored memory conflict information of the read re-ordered load check instruction further comprises passing control by the read re-ordered load check instruction to a next instruction in the instruction sequence." **[Kenner discloses this limitation e.g. in column 15, lines 14-22]**

With respect to **claim 21,**

"The computer system of claim 18, further comprising a bus **[See FIG. 3, element 315, "Bus"]** *to control communications* **[Kenner discloses in column 9, lines 53-55, "The bus 315 represents one or more busses (e.g., PCI, ISA, X-Bus, EISA, VESA, etc.) and bridges (also termed as bus controllers)."]** *between the processor* **[See FIG. 3, element 305, "Processor"]** *and the memory device."* **[See FIG. 3, element 310, "Storage Device"]**

With respect to **claim 23,**

"The machine-readable medium of claim 22, the sequence of instructions **[Kenner discloses in the abstract, "sequences of instructions"]**, *when executed by the computer system* **["When executed by a computer system, the sequences of instructions cause the computer system to perform a series of steps..."]**, *further causing the computer system to validate stored memory conflict information ~~with a~~ having the matching address if the stored memory conflict information has ~~the same~~ a different data value as than the value of the potentially conflicting load."* **[Kenner discloses this limitation in column 17, lines 9-14]**

[Note: With respect to claims 22-24, Kenner discloses a machine-readable medium in the abstract.]

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

1ST POINT OF ARGUMENT:

With respect to the arguments on page 10 of the applicant's remarks, the examiner respectfully disagrees with the applicant that Kenner does not disclose *or* suggest *validating the stored memory conflict information with a matching address to the address of the potentially conflicting load if the stored memory conflict information has a value that is the same as a data value of the potentially conflicting load*. **Kenner discloses this limitation in column 16, lines 36-45. The examiner notes that a valid bit can**

be used to either invalidate or validate a particular data item, depending on its setting. Additionally, Kenner discloses using the *same* data values of potentially conflicting loads when validating in column 19, lines 17-22.

Furthermore, the examiner cannot point to the exact location in the applicant's specification that clearly supports the amended claim by the applicant. Paragraphs [0042], [0043], [0045], and [0049] are cited by the examiner as supporting *parts* of the stated amended limitation, but are not clear in supporting the limitation as a whole. Examiner respectfully asks the applicant to point out in the specification where *"validating the stored memory conflict information with a matching address to the address of the potentially conflicting load if the stored memory conflict information has a data value that is the same as a data value of the potentially conflicting load"* is found within the applicant's specification.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone

numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy

Patent Examiner
Art unit: 2189

Reginald G. Bragdon

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